

(use as many sheets as necessary)

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of

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Application Number	09/802,405
Filing Date	March 9, 2001
First Named Inventor:	Wolf-Dietrich Weber
Art Unit	2126
Examiner Name	Siddiqi, Mohammad A.
Attorney Docket Number	002998.P013

[illegible]

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ^o
		Country Code ³ Number ⁴ Kind Code ⁶ (if known)				

**Examiner
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M. A. Seddyn

Date Considered

08/21/2008

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Substitute for Form 1449/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (as many sheets as necessary) JUL 30 2004 PATENT & TRADEMARK OFFICE		Application Number	09/802,405
		Filing Date	March 9, 2001
		First Named Inventor:	Wolf-Dietrich Weber
		Art Unit	2126
		Examiner Name	Siddiqi, Mohammad A.
Sheet 2 of 2	Attorney Docket Number	002998.P013	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T ²
MBS		GOOSSENS, KEES, et al., "Guaranteeing the Quality of Services in Networks on Chip," Philips Research Laboratories, Eindhoven, The Netherlands Technical University of Eindhoven, Eindhoven, The Netherlands, In Axel Jantsch and Hannu Tenhunen, editors, Networks on Chip, Kluwer, Chapter 4, March 2003, pp. 61-82.	
MBS		SGROI, M., et al., "Addressing the System-on-a-Chip Interconnect Woes Through Communication-Based Design," University of California at Berkeley, Princeton University, DAC 2001, June 18-22, 2001, Las Vegas, Nevada, (7 pgs).	

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Examiner Signature	M. A. Siddiqi	Date Considered	08/21/2006
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Application Number	09/802,405
Filing Date	March 9, 2001
First Named Inventor	Wolf-Dietrich Weber
Art Unit	2154
Examiner Name	Mohammed A. Sidiqui
Attorney Docket Number	2998P013

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U.S. PATENT DOCUMENTS

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MAS		ZHANG, HUI, "Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks", Proceedings of the IEEE, Vol. 82, No. 10, October 1995, pp. 1374-1396.	
MAS		STILIADIS, DIMITRIOS et al., "Latency-Rate Servers: A General Model for Analysis of Traffic Scheduling Algorithms", In Proceedings of IEEE INFOCOM 96, April 1996, pp. 111-119.	
MAS		WINGARD, DREW, "Integration Architecture for System-on-a-Chip Design", IEEE 1998 Custom Integrated Circuits Conference, May 1998, pp. 85-88.	
MAS		WEBER, WOLF-DIETRICH, "Enabling Reuse via an IP Core-centric Communications Protocol: Open Core Protocol", In Proceedings of the IP 2000 System-on-Chip Conference, March 2000, pp. 1-5.	
MAS		WINGARD, DREW, "Sonics SOC Integration Architecture", Sonics, Inc., P1500 Presentation 1999, 25 pgs., www.OCP-IP.org.	
MAS		WEBER, WOLF-DIETRICH, "Efficient Shared DRAM Subsystems for SOCs", Sonics, Inc., June 2001, 6 pages.	
MAS		WINGARD, DREW "A Non-Blocking Intelligent Interconnect for AMBA-Connected SoCs", Sonics, Inc., CoWare Arm Developer's Conference, October 6, 2005, 39 Pages.	
MAS		WEBER, WOLF-DIETRICH, "A Quality of Service Mechanism for Interconnection Networks in System-on-Chips", 1530-1591/05, 2005 IEEE, pp. 6 total.	

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